YUNTANG 韵唐

SPECIFICATION FOR QLED LCM

☐ Preliminary Specification

☑ Final Specification

韵唐 QLED

Customer Approve:

QC 品质:

R&D 研发:

Approved 批准:

产品型号(Description): YT129IBLXL004-A

项目编号(Project): QB129

Compile by 编制:	Quality/Engineer 品质/工程:	Checked 审核:	Approved 批准:
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REVISION RECORD

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1.0 General description

1.1 Introduction

YT129IBLXL004-A is QLED model a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel, a driving circuit and a back light system. This TFT LCD has a 12.95 (10:16) inch diagonally measured active display area with FHD(1200 horizontal by 1920 vertical pixel array) resolution. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type.

1.2 Features

- **4 lanes MIPI Interface**
- Data enable signal mode
- 8-bit color depth,display 16.7M colors
- Low driving voltage and low power consumption
- ROHS Compliant

1.3 General information

Item		Specification	Unit	Remarks
Outline Dimension(总成）		192.85(H) x 299.85(V) x 11.4(body)	mm	Tolerance:±0.2mm
Outline Dimension（LCM）		190.47(H) x 291.56(V) x 5.2(body)	mm	Tolerance:±0.3mm
Display area		174.31(W) x278.9(H)	mm	
Number of Pixel		1200(H) x RGB x 1920(V)	pixels	
Pixel pitch		0.1692(H) x 0.1692(V)	mm	
Pixel arrangement		Pixels RGB stripe arrangement		
Display mode		Normally Black		
Surface treatment		IPS Film		
Weight		TBD (Typ.)	gram	
Back-light		Single LED (Side-Light type)		
Power Consumption	B/L System	TBD	watt	
Driver IC		FT8201P		*Using IC
Polarizer : zhuyou		Up: 0° Down 90°	pcs	

1.4 Mechanical Information

Item		Min.	Typ.	Max.	Unit
Module Size	Horizontal(H)	190.17	190.47	190.77	mm
	Vertical(V)	291.26	291.56	291.86	mm
	Depth(D)	4.9	5.2	5.5	mm

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2.0 ABSOLUTE MAXIMUM RATINGS

2.1 Electrical Absolute Rating (GND=AGND=0V)

Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
Interface Supply Voltage	IOVCC	-0.3	-	+3.6	V	
Logic Supply Voltage	VCI	-0.3	-	+6.6	V	
Analog Supply Voltage	VCIP	-0.3	-	+6.6	V	
High speed interface Supply Voltage	VCCH	-0.3	-	+6.6	V	
Positive Voltage input	AVDD	-0.3	-	AVDD+ 0.5	V	
Negative Voltage input	AVEE	0	-	-6.6	V	
Power Supply Voltage	VGH	-0.3	-	+25	V	
Power Supply Voltage	VGL	0	-	-16	V	
Operation Temperature	TOPR	-20	-	+70	℃	
Storage Temperature	TSTG	-30	-	+80	℃	

Note: (1) All of the Voltages listed above are whith respective to GND=0V.

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2.2 TFT LCD Power Supply Voltage

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VCI	-	-	-	V
	AVDD	9	10	11	V
	AVEE	-	-	-	V
	IOVCC	1.7	1.8	1.9	V

2.3 Back-light Unit

Parameter	Symbol	Min	Typ	Max.	Unit	Note
LED Current	I_L	180	240	280	mA	Ta=25℃
LED Voltage	V_L	-	19.2	-	V	Ta=25℃
LED Life-time	h	20000	-	-	V	Ta=25℃，If=20mA

2.4 Environment Absolute Rating

Item	Symbol	Min.	Max.	Unit	Note
Operating Temperature	Topa	-20	70	℃	
Storage Temperature	Tstg	-30	80	℃	

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3.0 OPTICAL CHARACTERISTICS

3.1 Optical Specifications

Item	Symbol	Temp	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle range	Horizontal	θ_L	CR > 10	80	85	--	Deg	Note (1,2)
		θ_R		80	85			
	Vertical	θ_U		80	85	--	Deg	
		θ_D		80	85			
Luminance Contrast ratio		CR	θ = 0°	1200	1350	--	--	Note (1,2)
Brightness		YL		400	450	--	Cd/m2	Note (4,5)
Transmittance		T(%)	θ = 0°	3.5	3.9	--	%	
Color Gamut (C light)				--	110	--	%	
Reproduction of color （C-light）	White	Xw	θ =0°	-0.02	0.301	+0.02		Note (1,4)
		Yw			0.336			
	Red	Rx			0.657			
		Ry			0.327			
	Green	Gx			0.277			
		Gy			0.587			
	Blue	Bx			0.138			
		By			0.080			
Response Time (Rising + Falling)	Trt		Ta= 25° C θ = 0°	--	30	40	ms	Note (1,3)
Opetical View Direction			ALL					Note (1)

3.2 Measuring Condition

Measuring surrounding: dark room
Ambient temperature: 25±2℃
15min. warm-up time.

3.3 Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-7 for other optical characteristics. Measuring spot size: 20 ~ 21 mm

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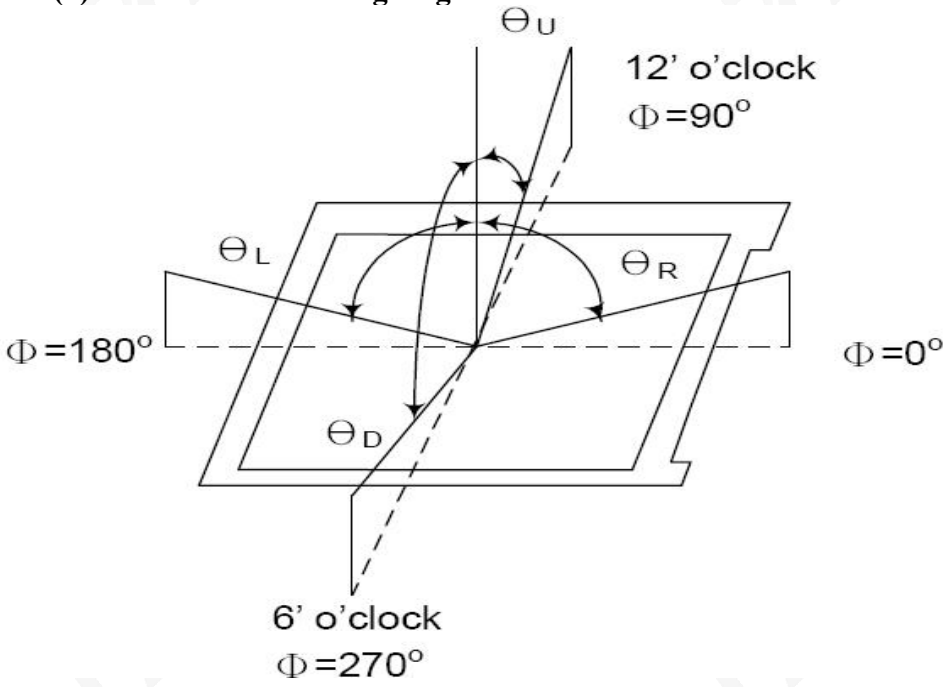
Note (1) Definition of Viewing Angle :

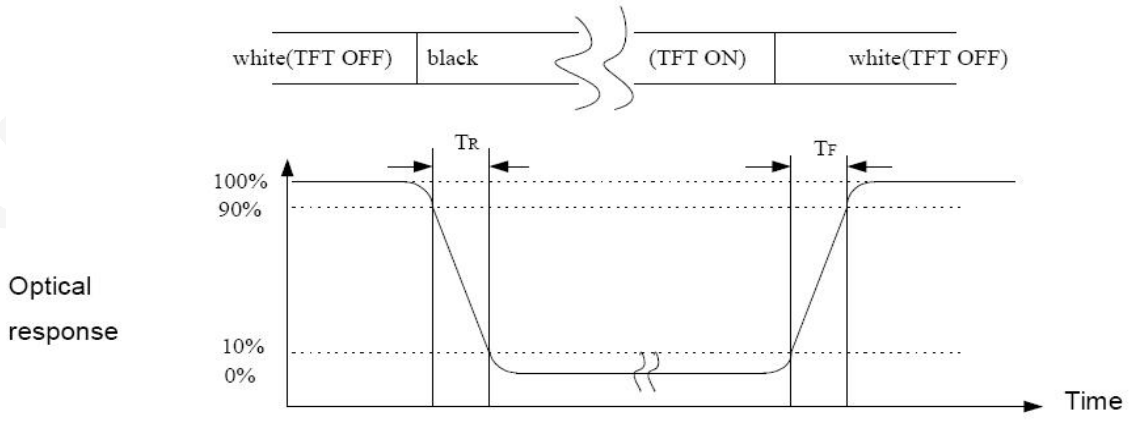


Note (2) Definition of Contrast Ratio (CR):

Measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3) Definition of Response Time: Sum of TR and TF



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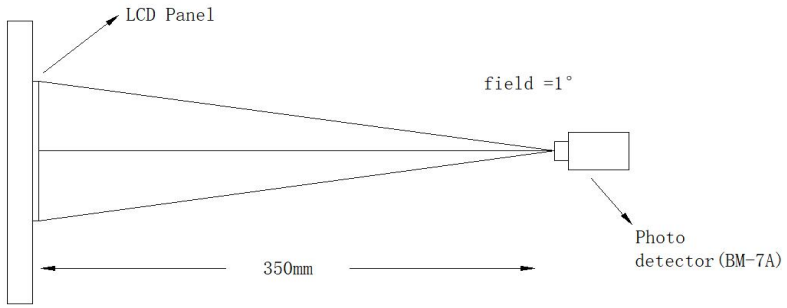
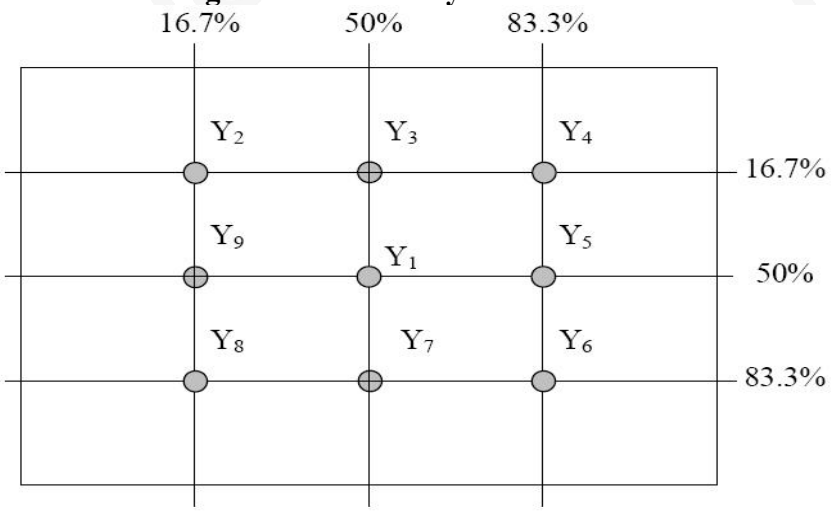
Note (4) Definition of optical measurement setup



Note (5) Definition of brightness uniformity



$$\text{Luminance uniformity} = \frac{\text{(Min Luminance of 9 points)}}{\text{(Max Luminance of 9 points)}} \times 100\%$$

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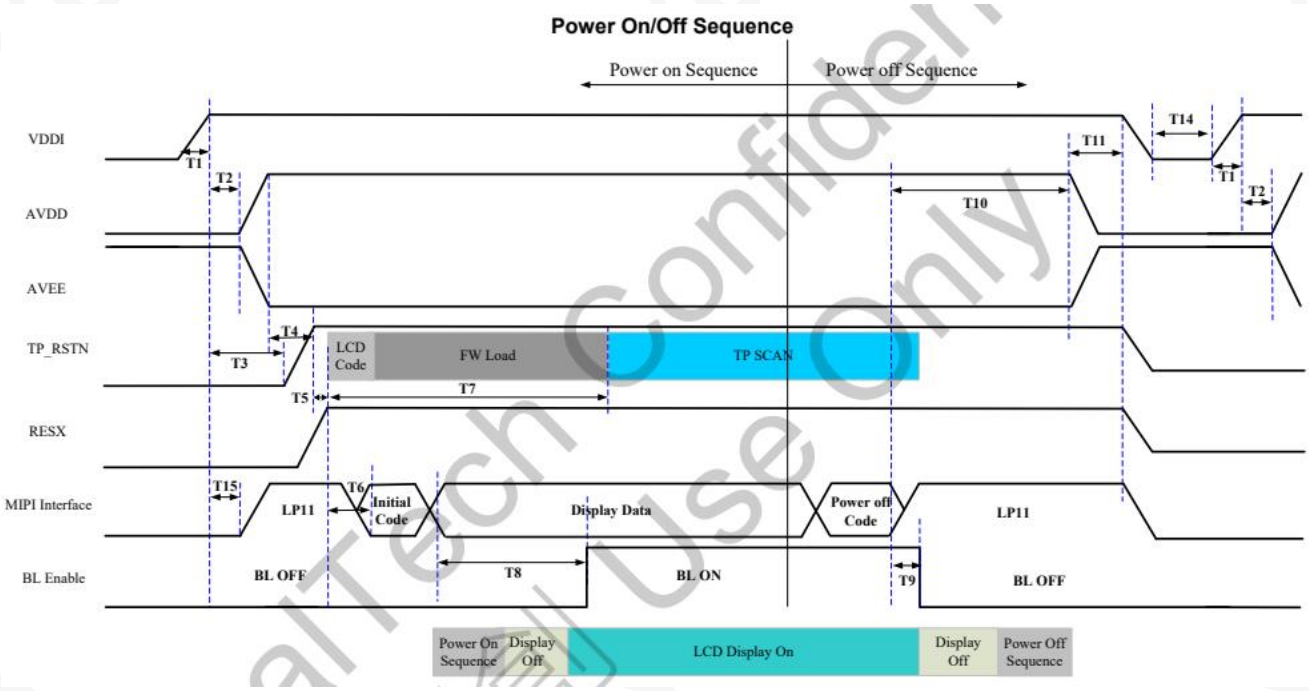
4.0 Power On/Off Sequence

To prevent the device damage from latch up,the power on/off sequence shown Below must be followed.

1. There will be no damage to the display module if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off sequences.
3. There will be no abnormal visible effects on the display between end of Power On sequence and before receiving Sleep Out command.
Also between receiving Sleep In command and Power Off sequence.
4. RESX and TP_RSTN must be held stablely by host during Power On Sequence, otherwise function is not guaranteed.
5. The display module can also initialize and calibrate DSI-CLK +/- and DSI-D0 +/- lanes within 5ms after LP-11 (Clock and Data Channels),
VDDI are applied and H/W Reset is not active (5ms is as same as the Reset Cancelling Time).
6. During Power off, VDDI can be powered down 5ms after AVDD/AVVEE power down if LCD in Sleep-In Mode.
7. During Abnormal power dropping, VDDI can start power down 5ms after AVDD/AVEE power down.
8. BL Enable timing is for reference only and not restricted (T8/T9).



TP Gesture Mode Exit Sequence

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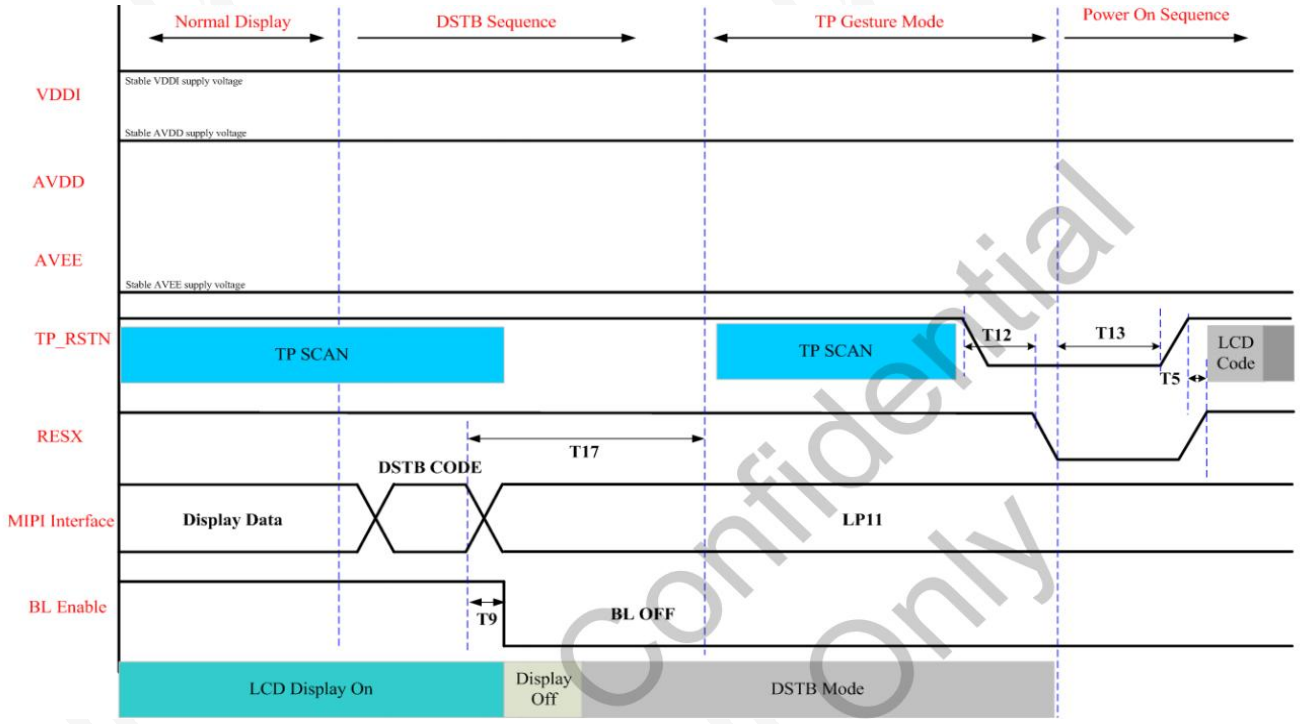
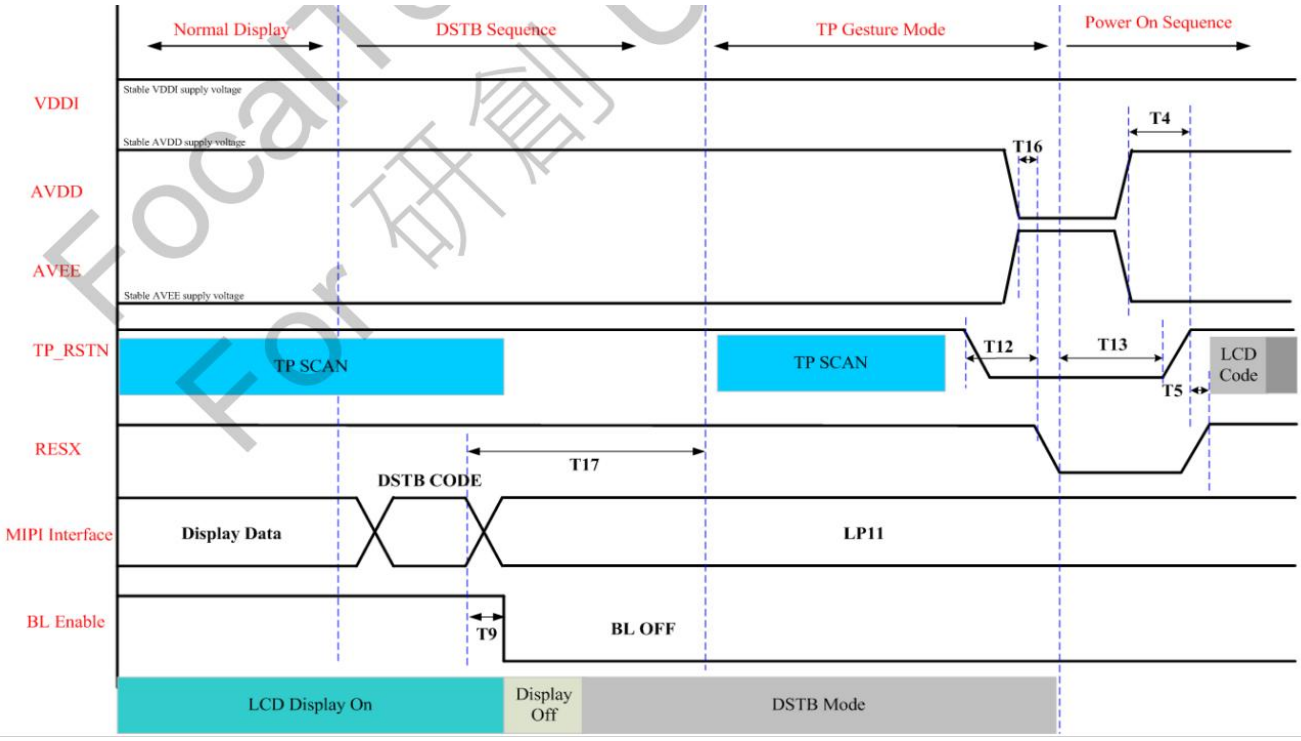


TP Gesture Mode Exit Sequence with AVDD/AVEE disabled



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Power On / Off Sequence Timing				
Parameter	Description	Min.	Max.	Unit
T1	Rise time from 0.1VDDI to 0.9VDDI	0	5	mS
T2	AVDD/AVEE rise after VDDI power on	3		mS
T3	TP reset time after VDDI power on	5		mS
T4	TP Reset release time after AVDD power on	100		uS
T5	TP Reset release to LCD Reset release	0		mS
T6	FLASH download LCD code after LCD Reset	35		mS
T7	LCD Reset release to TP SCAN Start (Single Chip application)	150		mS
	LCD Reset release to TP SCAN Start (Cascade application)	350		mS
T8	LED On after Initial Code	150		mS
T9	LED Off after power off code	50		mS
T10	AVDD/AVEE power down after power off code	150		mS
T11	VDDI power down after AVDD/AVEE power down	5		mS
T12	TP reset time before LCD reset	5		mS
T13	RESX reset falling to TP reset release	5	120	mS
T14	VDDI rise again after previous VDDI powered down	50		mS
T15	MIPI signals start (Hi-Z/GND to LP11) after VDDI power on	3		mS
T16	AVDD/AVEE power down to LCD reset	1		mS
T17	TP Gesture mode start after power off command code	150		mS
Trf	2nd LCD Reset time after TP_RST assert	5		mS
Trl	2nd LCD/TP Reset overlap time	5		mS
Trw	TP Reset High Level Width before 2nd Reset		10	mS

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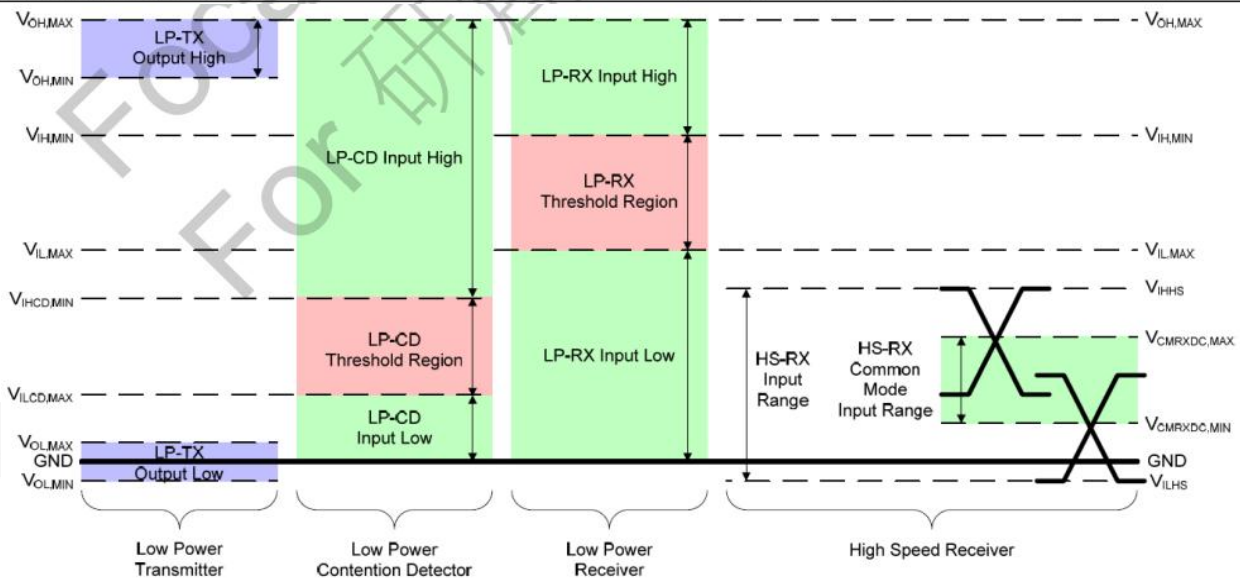
5.0 ELECTRICAL CHARACTERISTICS

5.1 DC characteristics for MIPI-DSI

(AVDD = 5.0V~6.5V,AVEE = -5.0V~-6.5V,VDDI = 1.65V~1.95V, Ta = -30°C ~ 70°C)

Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Power supply voltage for MIPI Interface						
Power supply voltage for MIPI interface	VDDAM	-	1.65	1.8	1.95	V
	LVDSVDD	-	1.125	1.3	1.5	V
LPDT Input Characteristics						
Pad signal voltage range	VI	-	-50	-	1350	mV
Ground Shift	VGNDSH	-	-50	-	50	mV
Logic 0 input threshold	VIL	-	0	-	550	mV
Logic 1 input threshold	VIH	-	880	-	LVDSVDD	mV
Input hysteresis	VHYST	-	25	-	-	mV
LPDT Output Characteristics						
Output low level	VOL	-	-50	-	50	mV
Output high level	VOH	-	1.1	1.2	1.3	V
Logic 1 contention threshold	VIHCD,MIN	-	450	-	LVDSVDD	mV
Logic 0 contention threshold	VILCD,MAX	-	0	-	200	mV
Output impedence of LPDT	ZOLP	-	80	100	125	ohm
Hi-speed Input/Output Characteristics						
Single-end input low voltage	VILHS	-	-40	-	-	mV
Single-end input high voltage	VIHHS	-	-	-	460	mV
Single-end threshold for HS termination enable	VTERM-EN	-	-	-	450	mV
Differential input low threshold	VIDTL	-	-70	-	-	mV
Differential input high threshold	VIDTH	-	-	-	70	mV
Common mode voltage	VCMRXDC	-	70	-	330	mV
Differential input impedence	ZID	-	80	100		ohm



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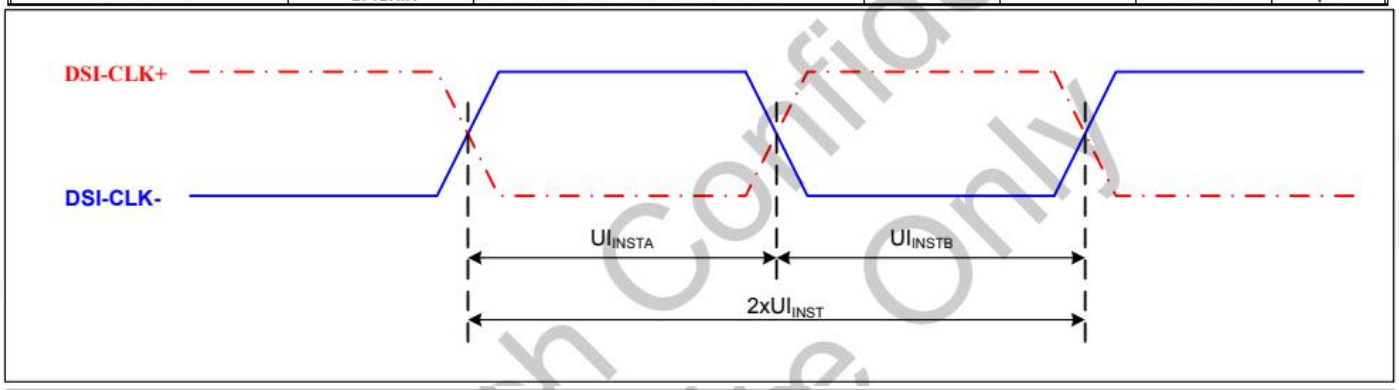
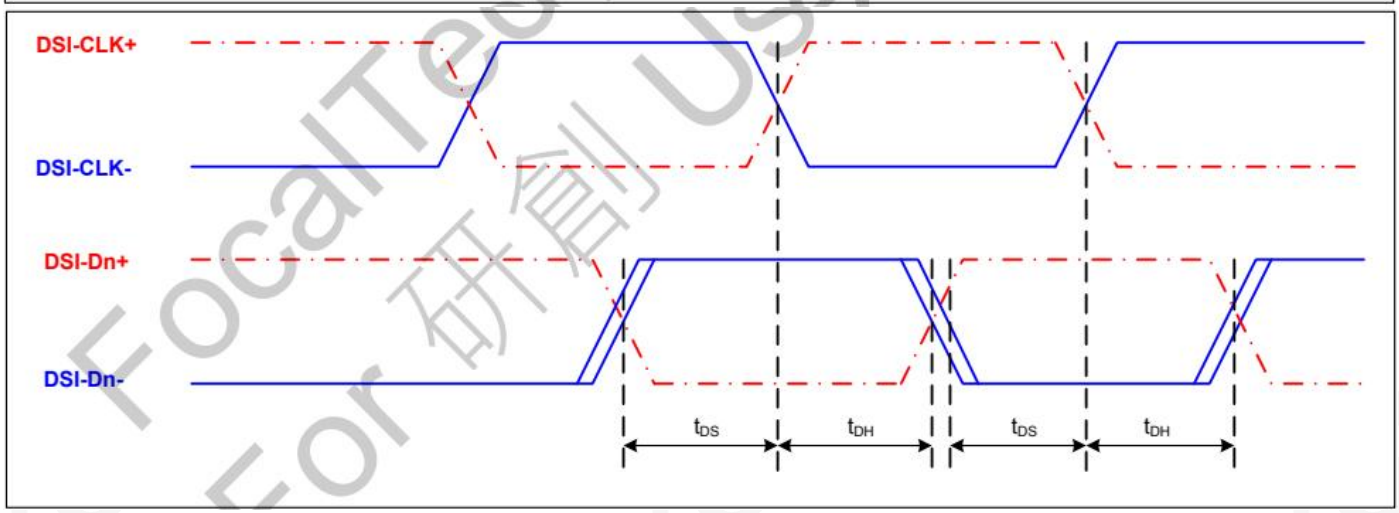
5.2 AC characteristics

MIPI-DSI characteristics

High speed mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Mode						
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	2	-	25	ns
DSI-CLK+/-	UI_{INSTA} , UI_{INSTB}	UI instantaneous Halfs	1	-	12.5	ns
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3UI	ps





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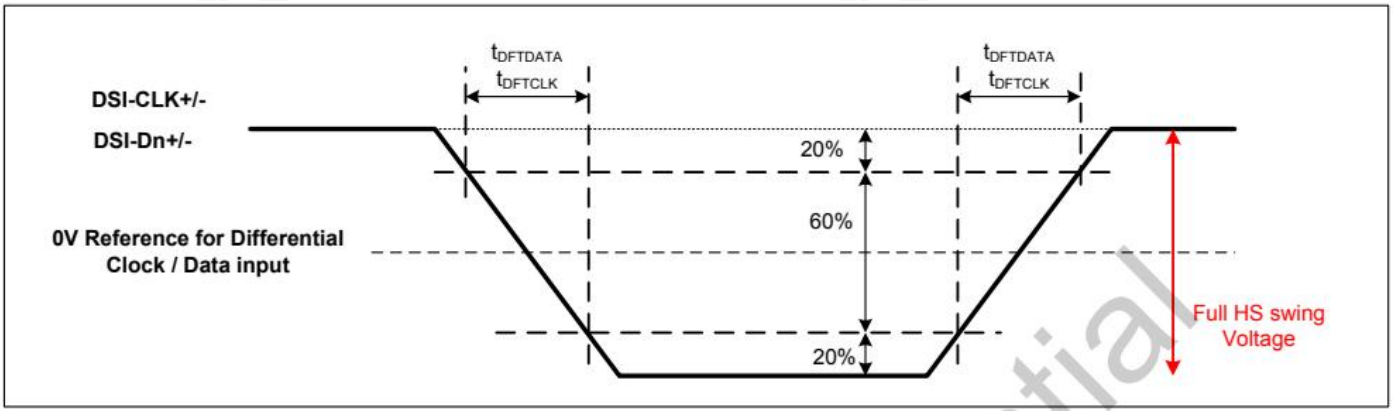

Figure: AC characteristics for MIPI-DSI High speed mode

Low power mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power mode						
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU Display Module	50	-	-	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module MPU	58	-	-	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2XT_{LPXD}$	ns
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	$5XT_{LPXD}$	-	-	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	$4XT_{LPXD}$	-	-	ns
DSI-D0+/-	Ratio T_{LPX}	Ratio of T_{LPXM} / T_{LPXD} between MCU and display module	2/3	-	3/2	-

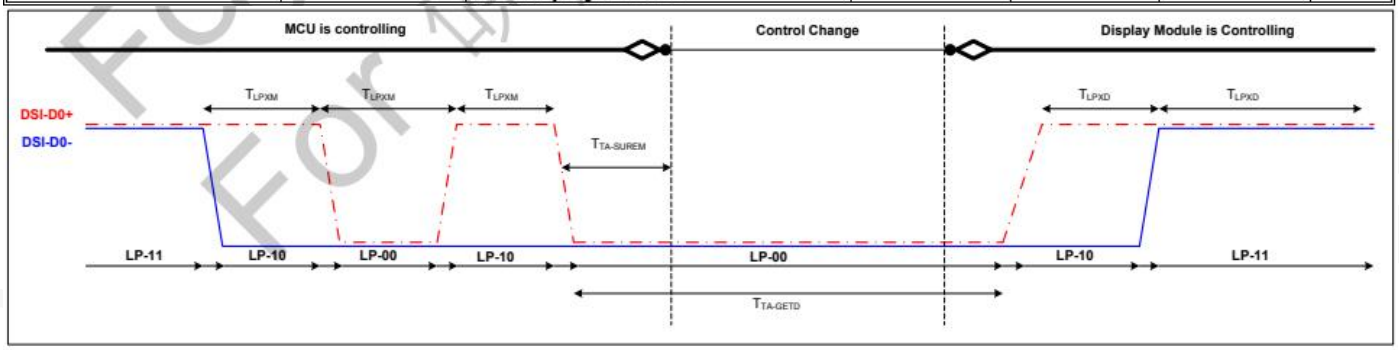

Figure: BTA from the MCU to the Display Module

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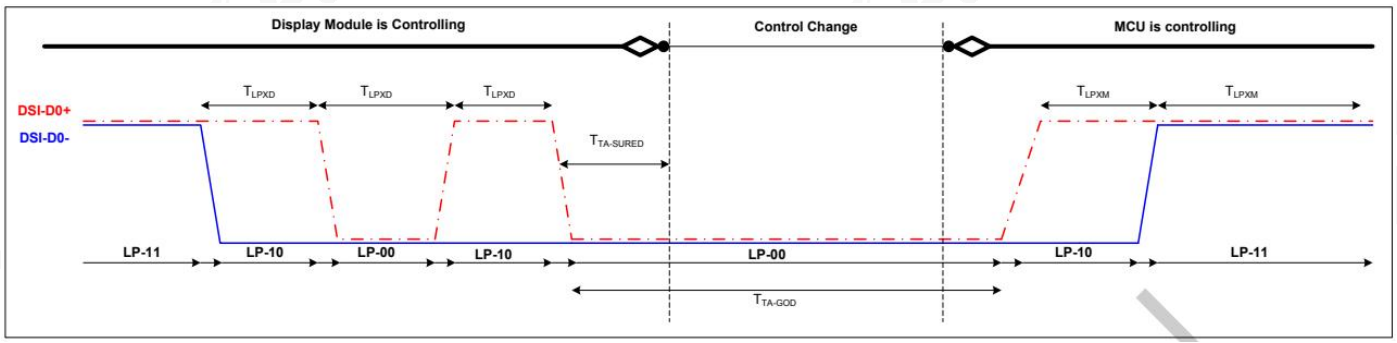

Figure: BTA from the Display Module to the MCU

Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	T_{LPX}	Length of any low-power state period	50	-	-	ns
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4UI	-	85ns + 6UI	ns
DSI-Dn+/-	$T_{HS-PREPARE}$ +$T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time to drive HS-0 before the sync sequence	145ns + 10UI	-	-	ns
DSI-Dn+/-	$T_{D-TERM-EN}$	Time to enable Data Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	35ns + 4UI	ns
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns + 4UI	ns
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns
DSI-Dn+/-	T_{EoT}	Time from start of $T_{HS-TRAIL}$ period to start of LP-11 state	-	-	105ns + 12UI	ns

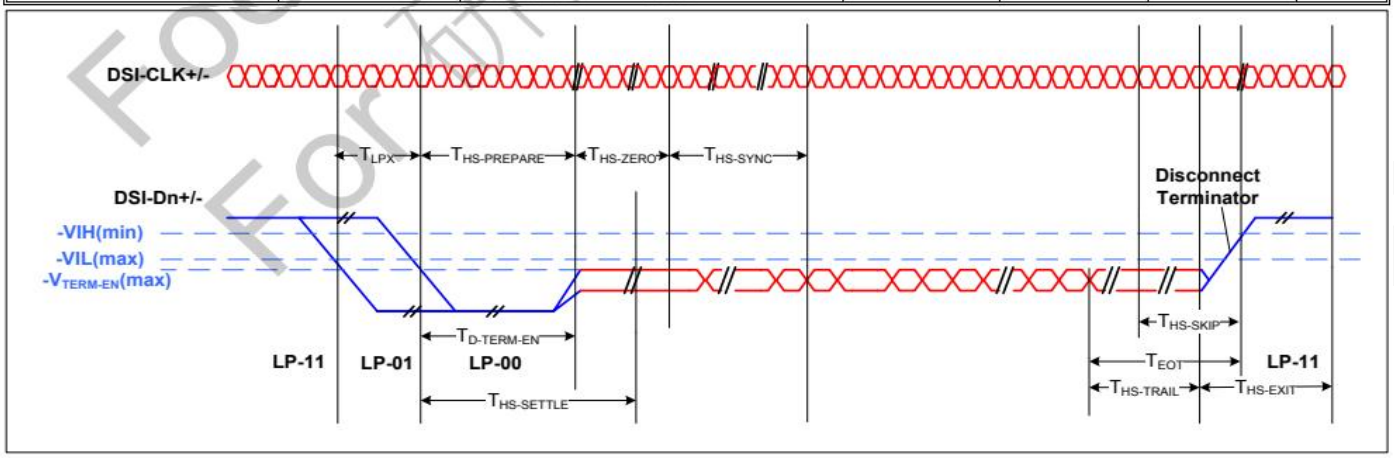

Figure: High Speed Data Transmission Bursts

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6.0 Reliability test items

Test Item	Test Conditions	Notes
High temperature Operation	Ta= +70℃, 96hrs	
Low temperature Operation	Ta= -20℃, 96hrs	
High Temperature Storage	Ta= +80℃, 96hrs	
Low Temperature Storage	Ta= -30℃, 96hrs	
Humidity Test	60℃ ,Humidity 90% ,96hrs	
Thermal Shock Test	-20℃,30min ~ +70℃,30min (30 cycle)	
Vibration Test(Packing)	Sine Wave 1.04G, 5~500Hz, XYZ 30min/each direction	
Static Electricity	Half-Sine, 100G, 6ms, ±XYZ, 3 cycle	

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7.0 INTERFACE PIN CONNECTION

TP of interface I2C 1.8V

Terminal No.	Symbol	I/O	Functions
1	TP_RST	P	TP_RST
2	NC	P	NC
3	GND	P	Ground
4	TP_INT	P	TP_INT
5	TP_SDA	P	TP_SDA
6	TP_SCL	P	TP_SCL

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LCM of interface

Terminal No.	Symbol	I/O	Functions
1	NC	P	No connection
2	IOVCC	P	Power for Digital Circuit（+1.8V）
3	IOVCC	P	Power for Digital Circuit（+1.8V）
4	NC	O	No connection
5	RESET	P	Global reset pin. Active Low to enter Reset State. Normally pull high. Connecting with an RC reset circuit for stability（+1.8V）
6	NC	I	No connection
7	GND	P	Ground
8	MIPI_D0-	I	Negative MIPI differential data inputs0-
9	MIPI_D0+	I	Positive MIPI differential data inputs0+
10	GND	P	Ground
11	MIPI_D1-	I	Negative MIPI differential data inputs1-
12	MIPI_D1+	I	Positive MIPI differential data inputs1+
13	GND	P	Ground
14	MIPI_CLK-	I	Negative MIPI differential clock inputs
15	MIPI_CLK+	I	Positive MIPI differential clock inputs
16	GND	P	Ground
17	MIPI_D2-	I	Negative MIPI differential data inputs2-
18	MIPI_D2+	I	Positive MIPI differential data inputs2+
19	GND	P	Ground
20	MIPI_D3-	I	Negative MIPI differential data inputs3-
21	MIPI_D3+	I	Positive MIPI differential data inputs3+
22	GND	P	Ground
23	NC	O	No connection
24	AVDD	P	Power for Analog Circuit(9-11V)
25	NC	O	No connection
26	NC	O	No connection
27	NC	O	No connection
28	NC	O	No connection
29	NC	O	No connection
30	GND	P	Ground

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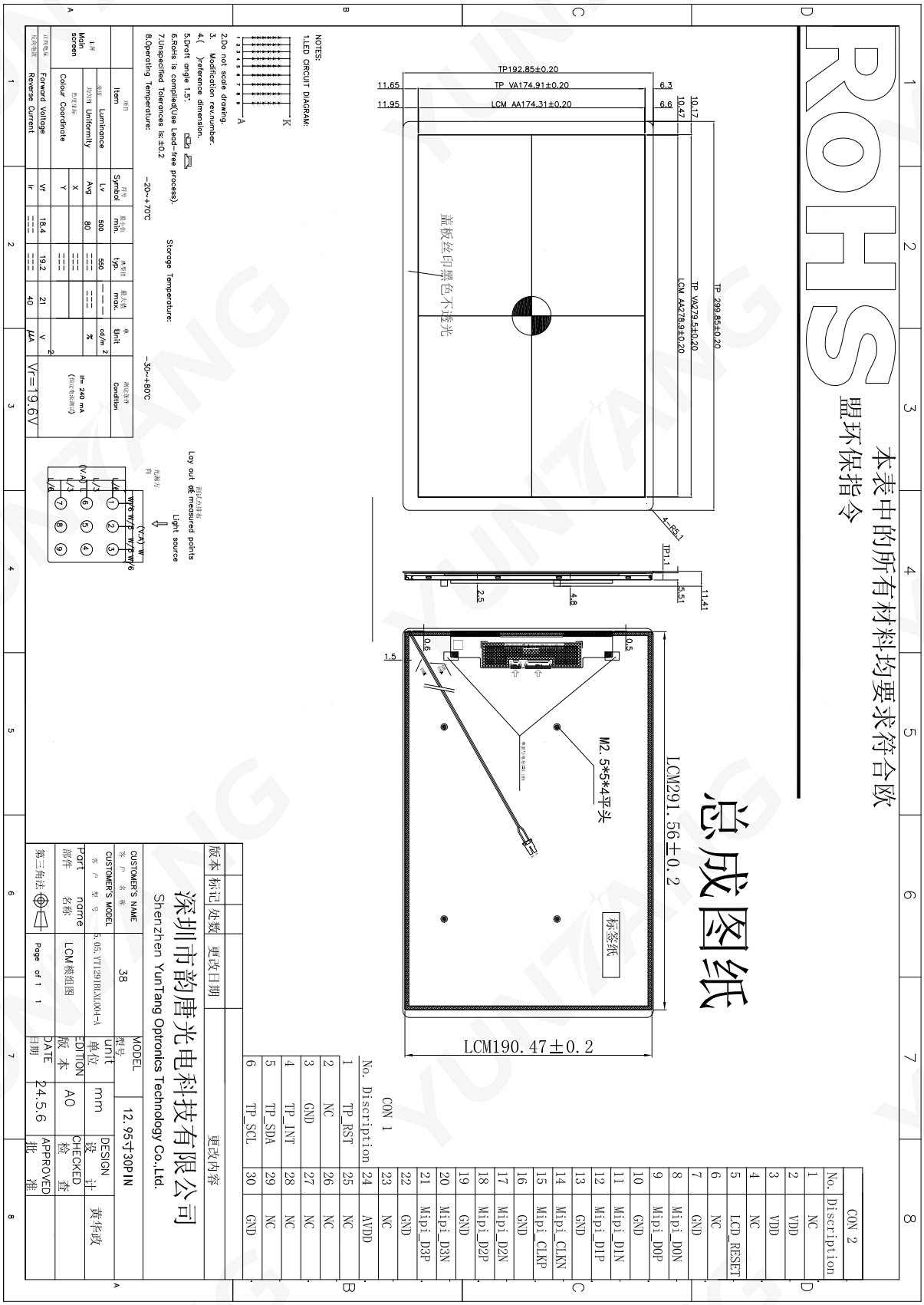
8.0 OUTLINE DIMENSION



No.	Discription
1	NC
2	VDD
3	VDD
4	NC
5	LCD_RESET
6	NC
7	GND
8	Mipi_DON
9	Mipi_DOP
10	GND
11	Mipi_D1N
12	Mipi_D1P
13	GND
14	Mipi_CLKN
15	Mipi_CLKP
16	GND
17	Mipi_D2N
18	Mipi_D2P
19	GND
20	Mipi_D3N
21	Mipi_D3P
22	GND
23	NC
24	AVDD

No.	Discription
1	TP_RST
2	NC
3	GND
4	TP_INT
5	TP_SDA
6	TP_SCL

Item	Symbol	min.	typ.	max.	Unit	Condition
Luminance	Lv	500	550	---	cd/m²	
Uniformity	Avg	80	---	---	%	
Main screen Colour Coordinate	X		---			If= 240 mA (指定电流测试)
	Y		---			
Forward Voltage	Vf	18.4	19.2	21	V	Vf=19.6V
Reverse Current	Ir	---	---	40	μA	

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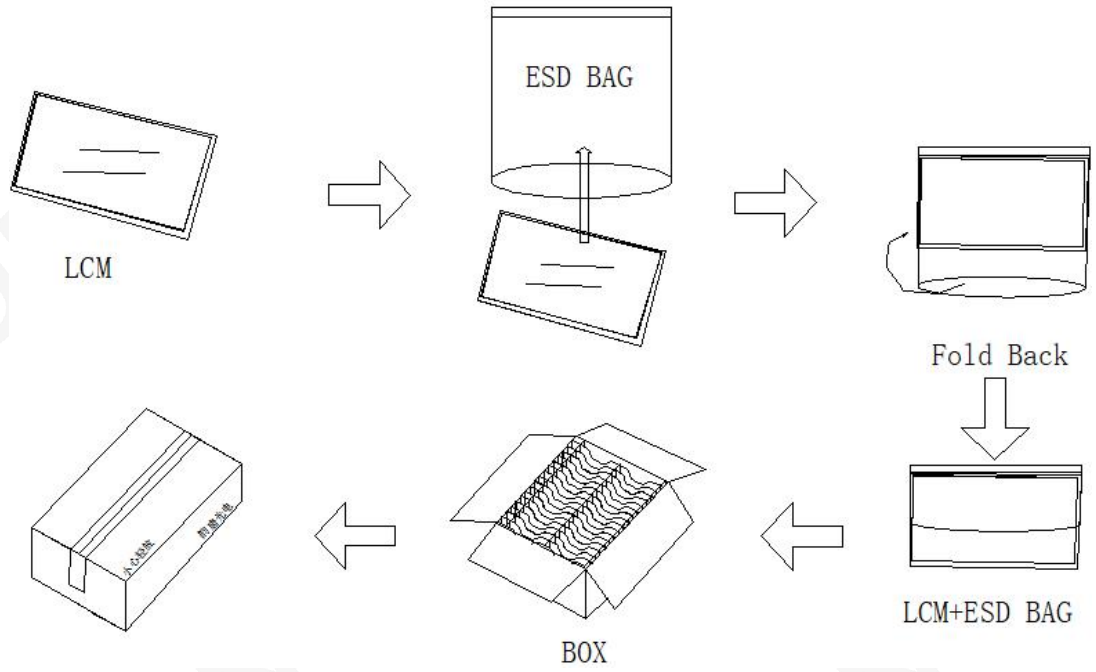
9.0 Pakcage Specification

9.1 Packing form

LCM Moudle	LCM Qty. in the box	Box size	Note
YT129IBLXL004-A	20 pcs/box		

9.2 Packing assembly drawing



	Material	Notice
Box	Corrugated Paper Board	(AB Flute)
Partition/Pad	Corrugated Paper Board	(B Flute)
Corner Pad	Corrugated Paper Board	(AB Flute)
ESD bag	PE	

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10.0 General precaution

10.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life threatening or otherwise catastrophic.

10.2 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. YT does not warrant the module, if customers disassemble or modify the module.

10.3 Breakage of LCD Panel

10.3.1.If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.

10.3.2. If liquid crystal contacts mouth or eyes, rinse out with water immediately.

10.3.3. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.

10.3.4. Handle carefully with chips of glass that may cause injury, when the glass is broken.

10.4 Electric Shock

10.4.1. Disconnect power supply before handling LCD module.

10.4.2. Do not pull or fold the LED cable.

10.4.3. Do not touch the parts inside LCD modules and the fluorescent LED's connector or cables in order to prevent electric shock.

10.5 Absolute Maximum Ratings and Power Protection Circuit

10.5.1. Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged.

10.5.2. Please do not leave LCD module in the environment of high humidity and high temperature for a long time.

10.5.3. It's recommended to employ protection circuit for power supply.

10.6 Operation

10.6.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead.

10.6.2 Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.

10.6.3 When the surface is dusty, please wipe gently with absorbent cotton or other soft material.

10.6.4 Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.

10.6.5 When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate solvent.

10.7 Mechanism

Please mount LCD module by using mouting holes arranged in four corners tightly.

10.8 Static Electricity

10.8.1 Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.

10.8.2. Because LCD module use CMOS-IC on circuit board and TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge. Persons who handle the module should be grounded through adequate methods.

10.9 Strong Light Exposure

The module shall not be exposed under strong light such as direct sunlight. Otherwise, display characteristics may be changed.

10.10 Disposal

When disposing LCD module, obey the local environmental regulations.

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